JFET AND MESFET STRUCTURES FOR LOW VOLTAGE, HIGH CURRENT AND HIGH FREQUENCY APPLICATIONS

This patent application is a Divisional patent application of commonly-owned patent application Ser. No. 11/121,381, filed on May 3, 2005 now U.S. Pat. No. 7,045,397, entitled "JFET AND MESFET STRUCTURES FOR LOW VOLTAGE, HIGH CURRENT AND HIGH FREQUENCY APPLICATIONS", by Yu et al., which is a Divisional patent application of commonly-owned patent application Ser. No. 10/153,012, filed on May 20, 2002 now U.S. Pat. No. 6,921,932, entitled "JFET AND MESFET STRUCTURES FOR LOW VOLTAGE, HIGH CURRENT AND HIGH FREQUENCY APPLICATIONS", by Yu et al., which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of semiconductor devices. More specifically, the field of the present invention is directed to junction field effect transistors (JFETS) and MESFETS for use in low voltage, high frequency and high current applications.

2. Related Art

The semiconductor industry faces difficult challenges in satisfying the expanding needs to provide transistors that are suitable for power management with low voltage applications, e.g., below 3 volts. As the feature size of the integrated circuits (ICs) become ever smaller and electronic devices are continuously being miniaturized, the voltages from AC or DC power sources that provide power to these devices are further dropped. Dropping the voltage from five volts to three volts results in a 25 percent reduction in power if the current density is maintained unchanged. At 1.8 volts, the power drops another 60%. However, the transient current loads can be very high. Under such operating conditions, 0.9 volts is the normal forward voltage drop for a p-n junction typically employed in a rectifier. Unfortunately, most of the power is consumed in the rectifying process. Therefore, power supply systems built with such types of p-n junctions are not really suitable for low voltage applications. Even the Schottky barrier diodes with a forward voltage drop below 0.5 volts are not a suitable solution to provide rectifiers or power switching devices for operation under the low voltage conditions.

Junction field effect transistors (JFETs) were developed after the invention of the bipolar transistors. A JFET transistor can be operated at very high frequencies with high switching speeds because the JFET transistor is operated with majority carriers. The depletion mode JFET transistor is well known and employed commonly in a naturally on state when the gate bias is zero. Because of the naturally on state, the JFET transistors are not as widely used in the semiconductor industry as the MOSFET, e.g., the metal oxide semiconductor field effect transistors. In order to make the JFET transistor operate in a naturally off state, the distance between the gates has to be reduced for the depletion regions from the gate to shut off the current conducting paths. However, such naturally off JFET transistors are not very useful in conventional configurations due to the longer current channel thus limiting the current capacity with a high on-resistance. S. M. Sze in "Physics of Semiconductor Devices" disclosed one example of such a configuration (Wiley & Son, 1981 Second Edition, page 322). The normally off JFET transistors discussed by Sze are for high

speed low power applications. The long current channel and high-on resistance limit the usefulness of JFET transistors particularly the high on-resistance prevents such transistors for use in applications in modern electronic devices operated with extremely low voltages.

FIG. **1** illustrates a conventional JFET structure **10** having a drain (D) region **16** and an source (S) region **14** which are implemented as wells within a substrate **12**. The gate (G) region **18** is also shown. A problem with this conventional JFET structure **10** is that it has a very long channel length thereby creating a large channel resistance. Further, the structure **10** consumes a large substrate surface area because the device **10** is substantially horizontal in orientation with respect to the surface of the substrate. Moreover, the drain **16** and source **14** contacts consume a relatively large amount of space on the substrate **12**. Further, gate diffusion is very difficult to control in the JFET structure **10** meaning that the threshold voltage, Vt, is difficult to control.

Moreover, in U.S. Pat. No. 4,523,111 entitled "Normally-Off Gate-Controlled Electric Circuit with Low On-Resistance", Baliga disclosed a JFET serially connected to an IGFET. The gate of the IGFET is operated as the gate for the serially connected circuit. The gate of the IGFET is applied to block the current to flow through a normally on JFET until the IGFET is turned on with a positively biased voltage above an IGFET threshold voltage. The on-resistance is the sum of the JFET resistance and the IGFET resistance. The on-resistance would not be adequate for extremely-low voltage applications required by modern electronic devices as discussed above. A similar invention is disclosed in U.S. Pat. No. 4,645,957 that is entitled "Normally Off Semiconductor Device with Low On-Resistance and Circuit Analogue" by Baliga. The JFET transistor is serially connected to a bipolar transistor to achieve the normally off state. Again, the on-resistance is the sum of the bipolar resistance and the JFET resistance and becomes too high for extremely low voltage applications.

In U.S. Pat. No. 5,321,283 entitled "High Frequency JFET" Cogan et al. disclose a JFET for radio frequency (RF) operation at high frequency. The normally-on JFET transistors disclosed in this patent are operated with high voltage and therefore they are not suitable to satisfy the requirements of modern portable electronic devices that require extremely low voltage and relatively high current capacity. Similarly, in U.S. Pat. No. 5,618,688 entitled "Method of Forming a Monolithic Semiconductor Integrated Circuit having an N-Channel JFET," Ruess et al. disclose a normally on JFET transistor manufactured with BiCMOS processes. The JFET transistors disclosed in this patent are not suitable for low voltage and high current applications.

Therefore, a need exits in the art of design and manufacture of a transistor suitable for low voltage, high current and high frequency applications and a fabrication process that would address the above difficulties.

SUMMARY OF THE INVENTION

Accordingly, embodiments of the present invention are directed to JFETS and MESFETS suitable for low voltage, high current and high frequency applications. Embodiments of the present invention include transistor structures that comprise an oxide layer disposed under the gate region to reduce junction capacitance. Gate length can be very tightly controlled by according to the present invention by partially removing the bottom oxide layer and exposing windows into the substrate. Therefore, Vt can be very accurately controlled according the present invention. For normally off